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Description

Method for controlled synchronization to an astable clock
system, 'and reception unit corresponding thereto

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The present invention relates to a synchronization method
for a reception unit, where cyclically emitted
synchronization signals are transmitted to the reception
unit by a transmission unit, where the reception unit
10 supplies the synchronization signals to a first clock
transmitter, where the first clock transmitter outputs an
essentially stable number of clock signals between two
synchronization signals, and also a reception unit
corresponding thereto.

15   Such synchronization methods and the corresponding
reception units are known generally. They are used, among
other things, in fieldbus systems, e.g. in the PROFIBUS.
Such fieldbus systems are distributed control systems
which generally have a transmission unit (head assembly,
20 bus master) and a multiplicity of reception units
(slaves). The individual slave assemblies are usually
driven by virtue of the transmission unit transmitting an
instruction message to the reception units. Upon receipt
of the instruction message, the reception units output to
25 a controlled technical installation nominal values which
have been transmitted to them previously by the
transmission unit. At the same time, they read in from the
controlled technical installation actual values which they
subsequently transmit to the transmission unit. The
30 transmission unit then calculates new nominal values which
it transmits to the individual reception units, so that
the reception units are ready for the next instruction
message.
        The instruction messages are sent by the
35 transmission unit with equidistant timing. From the

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instruction messages it is therefore possible to derive
synchronization signals which can be used to synchronize
the reception units to the transmission unit.

5   In practice, some latitude in time remains between
transmission of the actual values read in to the
transmission unit and transmission of the nominal values
to the reception units, on the one hand, and transmission
of the next instruction message, on the other hand. This
latitude is generally used for "acyclic" messages. In this
10   context, delays by the acyclic messages may cause
individual instruction messages to be sent late. Reception
of such instruction messages sent late causes erroneous
resynchronization of the reception units. In many
applications, this erroneous resynchronization is not
15   critical.

In time-critical applications, on the other hand,
particularly when coupling interpolating drive axes, such
erroneous resynchronization cannot be tolerated. To
prevent it, a phase regulator has therefore been proposed
20   such that the reception unit supplies the synchronization
signals to the first clock transmitter via this phase
regulator in a phase locked loop, and, upon receipt of the
synchronization signals, the phase regulator ascertains
instantaneous phase errors and readjusts the first clock
25   transmitter such that the first clock transmitter outputs
a   nominal   number   of   clock   signals   between   two
synchronization signals. To achieve sufficient accuracy in
the synchronization with the transmission unit, it has
been proposed that the phase regulator integrate the
30   instantaneous phase errors to form an integration value,
and that the integration value be corrected to form an
integration fraction, the integration fraction being less
than one (cf. DE 19932635.5).

The phase regulator in the phase locked loop (PLL)
35   generates a stable clock signal essentially from a

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synchronization signal which is received via the fieldbus system and is subject to interference. If this synchronization signal received via the fieldbus system disappears permanently (e.g. no bus connection available

5   any longer), then the phase regulator continues to produce a stable clock signal, although without being able to synchronize itself to the synchronization signal on the fieldbus system.

If the synchronization signal received via the

10   fieldbus is permanently available again after some time (e.g. bus connection restored), this synchronization signal will generally be entirely asynchronous with respect to the stable clock signal produced by the phase regulator. If the phase regulator is stopped in this case,

15   the stable clock pulses produced by the PLL disappear. If the phase regulator is restarted again, the stable clock pulses produced by the PLL are again produced in synchronism with the synchronization signal received via the fieldbus.

20   This conventional procedure is problematical, however, in terms of requirements of various applications, such as the coupling of interpolating drive axes. The synchronous operation of various axes, e.g. in the case of numerically controlled machine tools or robots, is

25   dependent on the stable clock signal produced by the PLL. Actual values are stored in synchronism with this clock pulse, for example, and nominal values are output.

However, the result of the disappearance of the clock signal produced by the PLL is then that the machine

30   tool is no longer able to determine the position of its axes and that the machine operator needs to rereference his axes.

For this reason, it is desirable, from an application point of view, for resynchronization to be

35   able to be carried out without the stable clock pulses

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produced by the PLL disappearing.

Accordingly, resynchronization to the synchronization signal received from the fieldbus should be soft, i.e. should involve only a slight change in the
5   stable clock signal produced by the PLL.

It is the object of the present invention to provide a synchronization method for a reception unit which allows soft synchronization to an astable clock system, and also a reception unit corresponding thereto.
10   The present invention achieves this object by developing the synchronization method described in the introduction on the basis of the preamble of the main claim, such that

- the stable clock signals are used to drive a
15   second clock transmitter,

- where the second clock transmitter generates a second clock signal which is continuously present, even when the first stable clock signals are absent,

- where a phase difference arising between the first
20   clock transmitter and the second clock transmitter is compensated for by influencing the period duration of the second clock transmitter.

The result of soft synchronization is that the clock signals produced largely keep their period duration,
25   so that there is the assurance that applications called cyclically with this timing, such as software applications, can also be executed to the full extent. Since the clock signals largely maintain their period duration, the application also remains sufficiently
30   accurate. Particularly at points where timing is critical, such as speed calculations etc., great advantages are obtained here as compared with a closed loop control solution. The process of soft synchronization thus barely differs from the normal operating state of the machine.
35   In this context, it has been found to be

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advantageous if only slight changes in the period duration
of the second clock transmitter are made such that the
phase difference is continuously reduced within a
prescribed time period until the first and the second
5   clock signal are synchronous with one another. In this
way, the process of synchronization is particularly soft.

Synchronization is performed particularly
effectively if the period duration of the second clock
transmitter is influenced such that the shorter interval
10 between the phases of the two clock signals is reduced.

In accordance with another advantageous refinement
of the method according to the present invention, the
second clock transmitter is driven with a prescribed
standard period duration in the event of the first stable
15 clock signal being absent. This ensures that, even if the
synchronization signal disappears, autarchic operation of
the application is possible.

When a phase regulator, outlined in the
introduction, in a locked loop (PLL) is used to produce a
20 first stable clock signal, the invention can be
implemented particularly simply and effectively if
fluctuations in the period duration of the first clock
transmitter which are corrected by the phase regulator are
mapped onto the second clock transmitter.

25 In this context, it has been found to be
beneficial if the corrections in the period duration of
the first clock transmitter which are ascertained by the
phase regulator from clock pulse to clock pulse are taken
into account both in the first stable clock signal and in
30 the continuously present second clock signal.

Other advantages and details of the invention can
be found in the description below of an advantageous
exemplary embodiment and in conjunction with the figures.
In these, elements having the same functionality are
35 identified using the same reference symbols. The figures

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show basic illustrations, in which

Figure 1   shows a distributed control system,

Figure 2   shows a reception unit,

5   Figure 3   shows a phase locked loop with a controlled
             clock transmitter connected downstream, and

Figure 4   shows a timing diagram for the controlled
             synchronization.

10   In accordance with FIGURE 1, a distributed control
system has a transmission unit 1 and reception units 2
connected to one another by means of a bus system 3. The
transmission unit 1 cyclically transmits messages to the
reception units 2, which react to the received messages
15   accordingly. By way of example, the reception units 2 read
in   input   variables   from   a   controlled   technical
installation or application 4, and emit output variables
to the technical installation or application 4. This is
indicated in FIGURE 1 by the arrows between the reception
20   units 2 and the technical installation/application 4.
          Usually, the transmission unit 1 and the reception
units   2   communicate   on   the   basis   of   the   following,
cyclically executed scheme:
          First, the transmission unit 1 transmits to the
25   reception units 2 output variables which are intended to
be output to the technical installation/application 4. It
then transmits an instruction message to the reception
units 2. On transmission of the instruction message, the
reception   units   2   output   the   output   variables   to   the
30   technical installation 4 and read in input variables from
the technical installation 4. The input variables read in
are then requested by the transmission unit 1.
          Ideally, the above scheme is executed strictly
cyclically and with strictly equidistant timing. In
35   particular, the instruction messages can therefore be used

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as synchronization signals S, or synchronization signals S
can be derived from the instruction messages. The
synchronization signals S can then be used to synchronize
the reception units 2 to the transmission unit 1.

5   On the basis of FIGURES 2 and 3, the
synchronization signals received by the reception units 2
are supplied via a bus connection module 2' to a phase
regulator 5 in a phase locked loop 6. The phase locked
loop 6 has a clock transmitter 7. Within the clock
10   transmitter 7, a clock generator 8 produces primary clock
signals which are supplied to a frequency divider 9. At
the output, the frequency divider 9 outputs the divided
primary clock signals as clock signals. The clock signals
are supplied to a clock signal counter 10.

15   With ideal regulation of the clock generator 8,
the clock transmitter 7 outputs exactly one nominal number
$Z*$ of clock signals between two synchronization signals S.
However, the clock transmitter 7 generally outputs a
number Z of clock signals which differs from the nominal
20   number $Z*$. The phase regulator 5 therefore ascertains
instantaneous phase errors z upon receipt of the
synchronization signals, and then readjusts the clock
transmitter 7 such that it outputs the nominal number $Z*$
of clock signals between two synchronization signals S.
25   This is done as follows:

Before the start of synchronization, that is to
say before the first instantaneous phase error z is
ascertained, a control unit 11 first prescribes a start
signal for a driving unit 12. This driving unit then
30   drives the clock generator 8 in the clock transmitter 7.
When the clock signal counter 10 has counted the nominal
number $Z*$ of clock signals, the clock signal counter 10
transmits a signal to the driving unit 12. The driving
unit then stops the clock generator 8 again. The phase
35   locked loop 6 has thus been "biased", so to speak. Upon

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receipt of the next synchronization signal, which is
likewise transmitted to the driving unit 12, the driving
unit then starts the clock generator 8 again. This
increments the clock signal counter 10 again.

5   The reaching of the nominal number Z* and the
arrival of the next synchronization signal S are reported
to a primary clock counter 13. Upon the arrival of the
first of these two signals, the primary clock counter 13
is started; upon the arrival of the second of the two
10   signals, it is stopped. The count (which has an arithmetic
sign) of the primary clock counter 13 is thus a direct
measure of the error between the clocking of the clock
transmitter 7 and the periodicity of the synchronization
signals S.

15   Upon receipt of the first synchronization signal S
after the clock transmitter 7 has been restarted, the
count of the primary clock counter 13 is transmitted to
the control unit 11. The control unit uses it to calculate
a correction value for driving the clock generator 8, and
20   prescribes this correction value directly to the phase
regulator 5. This at least substantially corrects the
instantaneous phase error z detected during the first
synchronization cycle.

        In the further synchronization cycles, the primary
25   clock counter 13 is always controlled on the basis of the
synchronization signal S and the reaching of the nominal
number Z*. The primary clock counter 13 is started upon
the arrival of the first of these two signals and is
stopped upon the arrival of the second of these two
30   signals. The count of the primary clock counter 13 is
supplied to a comparator 14.

        The count on the primary clock counter 13 is
compared with a maximum error. If the count exceeds the
maximum error, a timeout counter 15 is incremented. In
35   this case, no error signal is output to the phase

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    regulator 5. The phase regulator 5 maintains its previous output signal.

    The primary clock counter 13 is usually started and stopped whenever a synchronization signal S is

5   transmitted. However, it is also possible for a validity signal G to be additionally transmitted to the phase locked loop 6 by the control unit 11. In this case, the primary clock counter 13 is started and stopped only if the validity signal G is present. It is also possible to

10   start and to evaluate the primary clock counter 13 with a phase offset with respect to the synchronization signal S.

    If the phase regulator corrects the instantaneous phase errors to form a proportional fraction, with the proportional fraction being less than one, the phase error

15   is corrected more quickly. This applies particularly when the proportional fraction is greater than the integration fraction.

    If the phase regulator readjusts the clock transmitter only when the absolute value of the

20   instantaneous phase error does not exceed a maximum error, delays in the synchronization signals as a result of acyclic messages do not cause erroneous readjustment of the clock transmitter.

    If a counter is incremented when the maximum error

25   is exceeded, it is possible to detect a permanent error in the communication between transmission unit and reception unit, in particular.

    If a control unit transmits a validity signal to the phase locked loop, and the synchronization method is

30   carried out only when the validity signal is present, it is necessary to ensure that the correct synchronization signals are used for synchronization.

    If a clock generator within a clock transmitter produces primary clock signals which are supplied to a

35   frequency divider whose output emits the divided primary

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clock signals as clock signals, it is certain that all the components arranged between the clock generator and the frequency divider are likewise synchronized in the correct phase.

5   If, before the first instantaneous phase error is ascertained, the clock transmitter outputs the nominal number of clock signals, is then stopped and is restarted upon receipt of the next synchronization signal, the reception unit is synchronized particularly rapidly upon 10   startup.

      If, upon receipt of the first synchronization signal after the clock transmitter has been restarted, the instantaneous phase error is at least essentially corrected and integration of the instantaneous phase 15   errors and correction of the integration value, and possibly also correction of the instantaneous phase error, are not carried out until after receipt of the second synchronization signal, synchronization at the start of the method is speeded up even further.

20   According to the invention, however, the stable clock signal Z produced by the phase regulator in the phase locked loop 6 (PLL) is used only as an intermediate signal b. For the actual application 4 operated on the bus system 3 by the reception unit 2, another continuously 25   present clock signal a is produced. This is done using a further clock transmitter 7' which, like the first clock transmitter 7, [lacuna] likewise via a clock generator 8' for producing second primary clock signals and a frequency divider 9' connected downstream. The output signals 30   therefrom are applied to a clock signal counter 10' connected downstream. The way in which these components work is thus essentially equivalent to that for the phase locked loop 6.

      The intermediate signals b at the output of the 35   first clock counter 10 in the phase locked loop 6 and the

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continuously present second clock signals a at the output
of the further clock counter 10' are supplied to a further
comparator A for ascertaining the difference between the
clock signals a for the application 4 and the stable clock
5 signals b from the phase locked loop 6. As the measurement
result, the difference c is supplied to a reporting unit C
as a measure of the phase difference between the two clock
signals a and b. This reporting unit reports when c
becomes zero, which means that the clock signal a for the
10 application 4 is synchronous with the phase locked loop 6
and hence with the synchronization signal of the bus
system 3.

In addition, the phase difference c is passed to a
control unit B. This control unit additionally receives
15 the regulator output d of the phase regulator 5 and also a
status signal e. The status signal e delivers information
relating to the state of the phase locked loop 6, whether
the PLL is locked and stable, or else not locked, astable,
turned off or during the startup phase. A further signal f
20 passed to the control unit B provides the request for
"soft" synchronization when needed.

The following manner of operation is now selected
for the control unit B:

If the status signal e signals that the PLL 6 is
25 not stable (not locked, turned off, startup phase etc.),
the clock generator 8' is driven with a prescribed
standard period duration. The clock generator 8 thus runs
decoupled from the PLL 6 and allows the application 4 to
continue to operate autonomously without interruption.
30   If, by contrast, the status signal e signals that
the PLL 6 is stable or locked, the clock generator 8' is
driven using the regulator output d of the phase regulator
5, i.e. like the phase locked loop 6. The clock signals a
and b are thus produced exactly equally, i.e. the phase
35 difference c remains constant even if the clock signal b

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has slight fluctuations in period duration.

If the comparator A detects a phase difference c between the first clock signal b and the second clock signal a, which is continuously present, for the
5   application 4, the request signal f is used to ask the control unit B to drive the clock generator 8' with a value which is slightly modified as compared with the regulator output d, so that the phase difference c is gradually reduced.

10   The slight change in the period duration of the clock signal a produced for the application 4 enables said clock signal a to be altered such that the phase difference c between the stable clock signal b produced by the PLL 6 and the clock signal a produced for the
15   application 4 is slowly ("softly") reduced until, after a certain time, the two clock signals a, b are synchronous or have been synchronized with one another. For this purpose, the phase regulator 5 needs to be turned on (again), i.e. needs to produce clock pulses. By
20   continuously measuring a phase difference between the stable clock signal b produced by the PLL 6 and the clock signal a produced for the application 4, this phase difference can be gradually equalized to zero at any time by specifically changing the period duration of the clock
25   signal a produced for the application 4.

If the phase difference is +1000 ns, for example, then the period duration is now shortened by 10 ns in each case, for example in 100 periods of the clock signal a produced for the application 4. This slowly and gradually
30   reduces this phase difference to zero ("soft synchronization").

Turning off the stable clock signal b produced by the PLL 6 and turning it on again thus has no effect on the clock signal a produced for the application 4. The
35   application 4 can be operated without interruption.

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     If - as in the exemplary embodiment - the first clock transmitter 7 is regulated by means of a phase locked loop 6, it is necessary to ensure that the measured phase difference c does not alter from measurement to
5 measurement on account of the control response of the PLL 6, so that the control unit B can drive the second clock transmitter 7' such that the phase difference c can be reduced specifically.

     To achieve this, the fluctuations in the period
10 duration of the stable clock signal b produced by the PLL 6 are also - on account of the unavoidable control response of the PLL 6 - mapped in the clock signal a produced for the application 4, provided that the phase regulator 5 is not currently turned off
15   This means that the corrections in the period duration which are ascertained from clock pulse to clock pulse by the PLL 6 are taken into account both in the stable clock signal b produced by the PLL 6 and in the clock signal a produced for the application 4. The phase
20 difference c thus remains constant if the control unit B forwards only the regulator output d to the second clock transmitter 7'.

     This relationship is shown in the illustration in FIGURE 4. To this end, various cases X, Y and Z are shown,
25 with the following signals being plotted above one another: received synchronization signal S, stable clock signal b produced by the PLL 6 and clock signal a, which is continuously present and is produced for the application 4.
30   Case X shows a situation in which the synchronization signal S is subject to slight jitter z (deviations from the ideal expected clock instant). This is indicated by virtue of the actual clock signal (unbroken line) being situated slightly to the side of an
35 ideal expected clock instant (shown dotted). The stable

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clock signal b generated by the PLL 6 is then situated
virtually exactly at the expected clock instant. The clock
signal a produced for the application 4 is then situated
to the side of the ideal exact clock instant with a
5   possibly constant phase difference c0.

In case Y1 or Y2, the synchronization signal S has
a large degree of jitter z. This means that the PLL 6
produces a severe internal control response d1 or d2 in
order to generate a clock signal b which is synchronous
10 with the synchronization signal S. This would now have a
negative effect on the clock signal a shifted by a phase
difference c, because the control response of the PLL 6
would mean that this phase difference c would not remain
constant, but instead would also change on the basis of
15 the control response of the PLL 6. However, since the
control unit B takes the regulator output d into account
when driving the second clock transmitter 7', the phase
difference c remains constant C0. The PLL control response
thus changes over to the application clock signal a.

20 By virtue of the oscillations at the regulator
output d now being mapped onto the final clock signal a
for the application 4 in cases Y1 and Y2, this clock
signal a now behaves in exactly the same way as the first
clock signal b from the PLL 6. This produces a defined
25 phase difference c between the clock signals a and b. The
two clock signals a, b thus appear identical and are
shifted in time with respect to one another merely by a
fixed phase shift. On the basis of these clock signals,
the "soft synchronization" described above can then take
30 place without difficulty.

In principle, the problem can also be solved by
virtue of the clock signal a produced for the application
4 being regulated directly to the received clock signal b
or to the synchronization signal S. However, this has the
35 following disadvantages:

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The "soft synchronization" needs to be carried out in the controlled variable of the regulator 5 (= corrections ascertained by the PLL) by a limiter. This nonlinearity complicates the control loop. Said

5   nonlinearity needs to be examined on the basis of closed loop control technology and taken into account in the control loop (e.g. using additional limiters in the integral component of the regulator).

In the application instance for a PROFIBUS, the

10 PLL 6 is designed for correcting phase differences of approximately 1 μs (order of magnitude of the maximum jitter). The control parameters of the PLL 6 are therefore set very slowly or "softly" in order to filter the jitter. The phase shifts c arising during "soft synchronization"

15 are situated in the ms range, however. This means that other, faster and hence "harder" control parameters would be needed first. Changeover between these two control parameter sets would again represent a further nonlinearity in the control loop, which in turn

20 complicates the control loop. This would again need to be examined on the basis of closed loop control technology, and the necessary consequences would need to be derived.

On the basis of closed loop control technology, it would be necessary to take account of the fact that the

25 phase differences c are situated in the order of magnitude of the clock period durations. Depending on the control response, the two clocks under consideration could "overtake" one another, which could result in jumps in the phase difference measurement A. This in turn represents a

30 nonlinearity whose consequences would need to be examined.

All these points represent increased levels of involvement with no advantage as compared with the open loop control solution in accordance with the present invention. Reducing the problem to an open loop controller

35 instead of a closed loop controller allows significant

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simplification by contrast.

The method according to the invention allows, in particular, even interpolating axes with distributed control to be driven with sufficient accuracy.

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